

Amendment and Response

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Serial No.: 09/812,157

Confirmation No.: 2941

Filed: March 19, 2001

For: METHODS FOR PATTERNING METAL LAYERS FOR USE WITH FORMING SEMICONDUCTOR DEVICES

In the Claims

Please amend claims 58, 66, 74, 83, 93, and 102. The amended claims are provided below in clean form. Pursuant to 37 C.F.R. §1.121, amended claims are also shown in Appendix A with notations to indicate changes made (for convenience, all pending claims are provided in Appendix A).

58. **(AMENDED)** A method for patterning a platinum layer in the fabrication of integrated circuits, the method comprising:

providing a substrate assembly including a surface;

B2 forming a patterned metal-containing adhesion layer on the surface, resulting in at least one exposed surface region of the substrate assembly;

forming platinum on the patterned metal-containing adhesion layer and the at least one exposed surface region of the substrate assembly;

annealing the substrate assembly including the patterned metal-containing adhesion layer and the platinum thereon, causing pooling of the platinum on the at least one exposed surface region of the substrate assembly; and

removing at least a portion of the platinum from the at least one exposed surface region of the substrate assembly resulting in a patterned platinum layer.

66. **(AMENDED)** A method for forming a discontinuous conductive layer in the fabrication of integrated circuits, the method comprising:

B3 providing a substrate assembly comprising a surface having at least one metal-containing adhesion region and at least one surface region;

forming a platinum layer on the surface of the substrate assembly;

annealing the substrate assembly including the platinum layer formed thereon, causing pooling of the platinum layer on the at least one surface region of the substrate assembly; and

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removing at least a portion of the platinum layer from the at least one surface region
resulting in a discontinuous platinum layer on the at least one metal-containing adhesion region.

74. (AMENDED) A method for forming a patterned platinum layer in the fabrication of integrated circuits, the method comprising:

providing a substrate assembly including a surface having a patterned metal-containing adhesion portion thereon;

depositing a platinum layer on the surface of the substrate assembly and the patterned metal-containing adhesion portion, wherein the platinum layer has a thickness of about 600 Å or less;

annealing the substrate assembly at a temperature of about 1100°C or less, causing pooling of the platinum layer on the surface of the substrate assembly; and

removing unadhered platinum from at least a portion of the surface of the substrate assembly such that a resulting patterned platinum layer has a configuration substantially that of the patterned metal-containing adhesion portion, wherein annealing the substrate assembly and removing unadhered platinum from the portion of the surface of the substrate assembly is performed prior to forming any other materials on the platinum layer.

83. **(AMENDED)** A method for use in forming a capacitor, the method comprising:

providing a substrate assembly, the substrate assembly including at least one surface; and
forming an electrode on the at least one surface of the substrate assembly, wherein
forming the electrode comprises at least forming a platinum electrode layer, wherein forming the
platinum electrode layer comprises:

forming a discontinuous metal-containing adhesion layer on the at least one surface;

forming a platinum layer on at least portions of the at least one surface of the substrate assembly and the discontinuous metal-containing adhesion layer;

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annealing the substrate assembly, causing pooling of the platinum layer on portions of the at least one surface of the substrate assembly; and

removing at least a portion of the platinum layer from the at least one surface of the substrate assembly resulting in a discontinuous platinum layer.

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93. **(AMENDED)** A method for forming a discontinuous conductive layer in the fabrication of integrated circuits, the method comprising:

providing a substrate assembly having a surface comprising at least one metal-containing adhesion region and at least one surface region;

forming a conductive metal layer on the surface of the substrate assembly, wherein the conductive metal layer comprises a metal different from a metal in the at least one metal-containing adhesion region;

annealing the substrate assembly including the conductive metal layer, causing pooling of the conductive metal layer on the at least one surface region of the substrate assembly; and

removing at least a portion of the conductive metal layer from the at least one surface region resulting in a discontinuous conductive metal layer on the at least one metal-containing adhesion region.

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102. **(AMENDED)** A method for patterning a platinum layer in the fabrication of integrated circuits, the method comprising:

providing a substrate assembly including a surface;

forming a titanium nitride layer on the surface of the substrate assembly;

patterning the titanium nitride layer to form a patterned titanium nitride adhesion layer on the surface, wherein patterning the titanium nitride layer results in at least one exposed surface region of the substrate assembly;

depositing a material comprising platinum on the patterned titanium nitride adhesion layer and the at least one exposed surface region of the substrate assembly;

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 annealing the substrate assembly including the patterned titanium nitride adhesion layer and the material comprising platinum, causing pooling of the material comprising platinum on the at least one exposed surface region of the substrate assembly; and

removing at least a portion of the material comprising platinum from the at least one exposed surface region of the substrate assembly resulting in a patterned platinum layer.
